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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/839,671	04/23/2001	Katsuaki Matsui	32011-171408	1009

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EXAMINER	
WEST, JEFFREY R	

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 04/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/839,671	MATSUI, KATSUAKI	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In view of the After Final Response filed on February 26, 2004, PROSECUTION IS HEREBY REOPENED. A new grounds of rejection is set forth below.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The Examiner does point out that Applicant's priority document contains six figures and a corresponding description of Figure 6 as conventional in the art. The instant application, however, does not contain a Figure 6 or the corresponding description (See JP Publication No. 2002-033455 and the corresponding translation provided).

Drawings

3. The appropriate corrected drawings were received on February 26, 2004. These drawings are acceptable.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable Japanese Publication No. 2000-030492 to Kurihara.

Kurihara discloses a semiconductor device having an access time measuring test mode comprising a circuit block to which an input signal is input at a timing in accordance with an input clock, and which outputs an output signal having a value corresponding to said input signal (0001 and Figures 1 and 2), a first signal path for guiding a test input signal, which has been supplied to a first terminal, to a signal input terminal of said circuit block ("ADO" in Figure 1), a second signal path for guiding a test clock, which has been supplied to a second terminal, to a clock input terminal of said circuit block ("CLK" in Figure 1), a third signal path for guiding a test output signal, which has been output from a signal output terminal of said circuit block, to a third terminal ("DO" through "2" and "TDO" in Figure 1), a fourth signal path for guiding said test clock, which is input to said clock input terminal, to a fourth terminal ("CLK" through "3" and "4" and "TCK" in Figure 1), wherein said third and fourth signal paths are formed so that wiring delay time of said third and fourth signal paths are substantially equal (i.e. the delay of flop-flop circuit "2" is controlled to be the same as the amount of delay in the delay circuit "4") (0014).

Although the invention of Kurihara does not specifically include pads for inputting and outputting the various signals, the Examiner takes Official Notice that it is very well-known in the art to include such signal pads for inputting and outputting signals (See for example, U.S. Patent No. 6,393,592 to Peeters et al., Figure 1B, "SI",

"CLK", and "SO"). Therefore, it would have been obvious to one having ordinary skill in the art to include signal pads to provide locations for measuring the signals in order to view the signal changes in determining the desired access time.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 22 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara in view of U.S. Patent No. 6,393,592 to Peeters et al.

As noted above, the invention of Kurihara teaches all of the features of the claimed invention except for providing selectors on the first and second signal paths in order to receive a test input during test operation and a non-test input during normal operation.

Peeters discloses scan flop circuitry and methods for making the same comprising a circuit block for connection to previous circuit blocks in a scan chain (column 4, lines 20-24) including a circuit block in which an input signal is input at a timing in accordance with an input clock and which outputs an output signal having a value corresponding to said input signal comprising a first signal path for guiding a test input signal to a signal input terminal of the circuit block, a second signal path

for guiding a clock to a clock input terminal of the circuit block, and a third signal path for guiding an output signal (Figure 3). Peeters also discloses a selector on the first signal path which, during normal operation, supplies an output signal from a preceding circuit block to the input terminal of the circuit block and which during a test operation supplies the test input signal to the signal input terminal of the circuit block as well as a selector on the second signal path which, during normal operation supplies a normal clock to the input terminal of the circuit black and during a test operation supplies a test clock to the clock input terminal of the circuit block (Figure 3 and column 4, lines 21-39). Peeters also discloses the conventional method of receiving and outputting the signals via test pads (Figure 1B, "SI", "CLK", and "SO").

It would have been obvious to one having ordinary skill in the art to modify the invention of Kurihara to provide selectors on the first and second signal paths in order to receive a test input during test operation and a non-test input during normal operation, as taught by Peeters, because, as suggested by Peeters, the combination would have provided increased flexibility in the use of the integrated circuit by allowing for operation in both functional and test modes (column 1, lines 31-34).

8. Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kurihara in view of Peeters and further in view of U.S. Patent No. 6,615,380 to Kapur et al.

As noted above, the invention of Kurihara and Peeters teaches all the features of the claimed invention except for providing selectors on the third and fourth signal

paths in order to supply a test output during test operation and a non-test output during normal operation.

Kapur teaches dynamic scan chains and test pattern generation methodologies comprising a plurality of circuit blocks connected in a scan chain wherein the path for guiding the test output signal from a signal output terminal includes a selector which supplies a test signal during testing and a normal output during normal operation (Figure 4 and column 2, lines 24-33).

It would have been obvious to one having ordinary skill in the art to modify the invention of Kurihara and Peeters to include providing a selector on the third signal path in order to supply a test output during test operation and a non-test output during normal operation, as taught by Kapur, because, as suggested by Kapur, the combination would have provided a method for selectively bypassing circuits during testing in order to use shorter test patterns resulting in a reduction in overall test data volume and test application time with the same quality of results (column 2, lines 24-33) and, similar to the motivation provided by Peteers, allowed the test data to be output to a first location during testing and allowed the functional data to be output to a different location during functional operation for two distinct operating modes

Although the combination of Kurihara, Peeters, and Kapur does not specifically disclose a selector on the fourth path (i.e. clock-to-out path) one having ordinary skill in the art would have been motivated to include such a selector since the combination of Kurihara, Peeters and Kapur teaches maintaining substantially no

delay between the third and fourth paths and placing a selector on both the third and fourth paths, instead of just the third path, would have insured that the signals on these two paths bypass the same sections of circuitry thereby maintaining equivalency and, similar to the motivation provided by Peteers, allowed the test clock to be output to a first location during testing and allowed the functional clock to be output to a different location during functional operation for two distinct operating modes.

Response to Arguments

9. Applicant's arguments with respect to claims 21-25 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

JP Publication No. 09-127205 to Nishiyama et al. teaches a measuring method for access time with differences in electric lengths corrected to reduce an error in access time measurement.

U.S. Patent No. 6,327,218 to Bosshart teaches an integrated circuit time delay measurement apparatus.

11. Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
April 1, 2004

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800